ABSTRACT OF THE DISCLOSURE

An arrangement of bump pads for use on a face of a flip-chip semiconductor die. The arrangement comprises four corner regions, each corner region comprising multiple I/O bump pads and power bump pads. The corner regions are specialized bump arrangements depending upon the size of the die, signal to power ratios, and the core power requirements. The die arrangement also comprises multiple edge regions having multiple I/O bump pads and power bump pads. The edge regions are located along the edges of the die and are interleaved between the corner regions. The dimensions of the corner regions and the edge regions depend upon the power to signal ratio of the region. Also provided is a core power region having multiple power bump pads, centrally located within the edge regions and the corner groups. Core requirements mandating an odd number of rows and columns of bumps for the core require a special "checkerboard" arrangement also provided. Connections between the bumps and the edge of the die surface are shown. According to a second embodiment, there is provided a die surface arrangement with two power bumps, one live voltage, or power, bump and one ground bump, and multiple I/O bumps, all bumps linearly aligned, with the ground and power bumps both located intermediate between the I/O bumps. The ground, power, and I/O bumps form an array, and this array is replicated linearly across the die surface forming a linear array arrangement having alternately directed redistribution traces. The die surface arrangement comprises multiple linear array arrangements interspersed with multiple linearly aligned core power bumps.